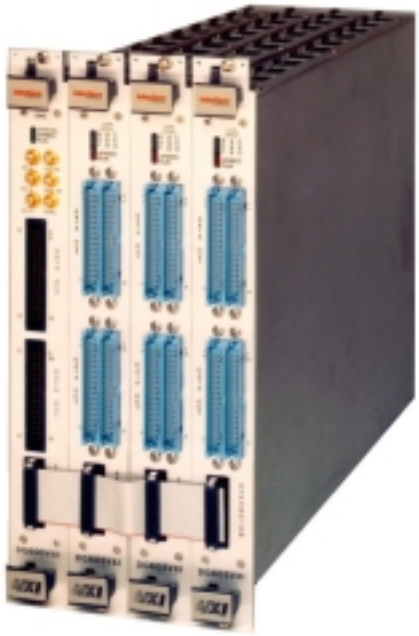
# DG600 / DG605

## VXI Digital Word Generator

## 25/50 MHz



- 16 to 112 Channels at 50 MHz with 16K Memory Depth
- 32 to 224 Channels at 25 MHz with 8K Memory Depth
- Independent Word Timing From 20 ns to 85 Seconds
- Internal Clock Rates From 1 Hz to 50 MHz, Up to 1 Hz Resolution
- Up to 255 Data Tables With 3 Level Nested Table Sequencing
- Clock-by-Clock Tristate Control For Each Channel
- IEEE-488.2 Common Commands and High Level VXI Bus Command Language

The DG600 is a message-based digital pattern generator implemented within a single slot, C-size module. It is capable of generating complex patterns at speeds up to 50 MHz while taking advantage of memory saving features such as three level looping and data tabling. There are 32 data channels available at speeds up to 25 MHz, and 16 of those channels will operate at speeds up to 50 MHz.

Up to three DG605 expansion modules can be used with the DG600. Depending on the number of DG605 units installed, the number of channels available in the 50 MHz operating mode is 16 to 112, in 32 channel increments. In the 25 MHz operating mode, 32 to 224 channels are available in 64 channel increments.

The DG600 and the DG605 provide tristate control for individual channels on a clock-by-clock basis, a feature essential for testing bidirectional busses often found in memory devices and microprocessor applications.

The DG600 implements the IEEE 488.2 common commands as a subset of a comprehensive, dedicated digital word generator command language. Sophisticated commands like "increment memory fills" allow quick set up of test conditions and data vectors. This saves time and cost by simplifying VXI software programming.

Timing of data output is supplied by a Phase-Locked-Loop (PLL) source, which allows selection of exact test frequencies from 1 Hz to 50 MHz with 1 Hz resolution. The PLL can be locked to either the 10 MHz VXI signal (CLK10), or to an external clock input. Triggering can be accomplished by either a user selected VXI trigger line or by providing an external trigger input. To efficiently provide mixed timing signals, the DG600 timing generator mode provides the exact time duration required for each word output, rather than running at a fixed clock speed which would otherwise require large amounts of memory.

When test vectors have an iterative nature, such as HDTV or Focal Plane Array testing, the DG600 uses data tables for optimum memory utilization. Data may be defined in up to 255 unique tables, which may be output in sequence as specified by the user. The data tables can be sequenced with up to three levels of nested looping.

The DG600 is equipped with a variety of clock outputs for synchronizing devices connected to the word generator. The ungated clock supplies a free running output based on the master clock source. The symmetrical clock output is a 50% duty cycle clock whose period matches the output word's time period. The gated symmetrical clock may be enabled or disabled on a word-by-word basis, making it useful as a data strobe for the UUT or as a sample clock for a data acquisition system.

# *DG600/DG605 SPECIFICATIONS**

| System Configuration | Speed MHz | No. of Channels | Memory Depth |
|---|---|---|---|
| DG600 only | 50/25 | 16/32 | 16K/8K |
| w/1 DG605 | 50/25 | 48/96 | 16K/8K |
| w/2 DG605 | 50/25 | 80/160 | 16K/8K |
| w/3 DG605 | 50/25 | 112/224 | 16K/8K |

## Internal Clock:

| | |
|---|---|
| Range | 20 ns to 1.3 ms (50 MHz mode)<br>40 ns to 85 sec (25 MHz mode) |
| Resolution | 1 Hz to 5 kHz |
| Frequency Stability | ± 0.1% |
| Phase Lock | CLK10 or Ext. 10 MHz |
| Sym. Clk. Duty Cycle | 50% ± 1 ungated clock cycle |

## External Clock:

| | |
|---|---|
| Range | 0 to 50 MHz |
| Minimum Pulse Width | 10 ns |
| Active Edge | Rising or falling |
| Input Voltage | 20 V p-p max., ± 10 V range |
| Input Threshold | Programmable ± 5.0 V, 20 mV resolution |

## External Trigger:

| | |
|---|---|
| Minimum Pulse Width | 10 ns |
| Active Edge | Rising or falling |
| Input Voltage | 20 V p-p max., ± 10 V range |
| Input Threshold | Programmable ± 5.0 V, 20 mV resolution |

## Channel to Channel Skew (typical values):

| | |
|---|---|
| Same Module | Less than 2 ns |
| DG600 to DG605 | Less than 6 ns |
| DG605 to DG605 | Less than 4 ns |

## Fixed Delays (typical values):

| | |
|---|---|
| Sym. Clk. to Data Out | 11 ns |
| Sym. Clk. to Sync | Less than 2 ns |
| Ext. Clk. to Sym. Clk | 30 ns |
| Ext. Trig. to Sym. Clk | 34 ns + 1 to 2 Clk |
| VXI Trig. to Sym. Clk | 31 ns + 1 to 2 Clk |

## Tables and Looping:

| | |
|---|---|
| Max. Active Tables | 255 |
| Min. Table Duration | 80 ns |
| Major Loops | 1 to 65,535 or continuous |
| Middle Loops | 1 to 65,535 or continuous |
| Minor Loops | 1 to 65,535 or continuous |

## Outputs:

| | |
|---|---|
| Type | FTTL (74F125) |
| Source | 12 mA minimum |
| Sink | 64 mA minimum |

# VXI Specifications

## Interface Compatibility:

| | |
|---|---|
| Type | Message-based, servant-only |
| Configuration | Static or dynamic |
| Revision | 1.3 and 1.4 |
| Size | C-size, single slot |
| Interrupt Level | Programmable 1-7 |
| Memory | A24/D16 only |
| Triggers | TTLTRG 0-7 |

## Power Requirements:

| | DG600 | | DG605 | |
|---|---|---|---|---|
| +5.0 V | 8.2 A | 41 W | 4.0 A | 20 W |
| -5.2 V | 50 mA | .26 W | - n/a - | - n/a - |
| +24.0 V | 20 mA | .48 W | - n/a - | - n/a - |
| -24.0 V | 10 mA | .24 W | - n/a - | - n/a - |
| -2.0 V | 25 mA | .05 W | - n/a - | - n/a - |
| | | -------- | | ------- |
| Total Power | | 42.03 W | | 20 W |

## Cooling Requirements:

| | |
|---|---|
| Per-Slot Average | 42 W (DG600)<br>20 W (DG605) |
| Airflow, DG600 | 3L/sec @ 0.3 mm water pressure for 10º C temperature rise (typ) |
| Airflow, DG605 | 2L/sec @ 0.3 mm water pressure for 10º C temperature rise (typ) |

## Environmental Specifications:

| | |
|---|---|
| Temperature | Storage = -40 Cº to +75 Cº<br>Operating = 0º C to +45º C |
| Humidity | 5% to 95% relative, noncondensing |

## Software Drivers:

| | |
|---|---|
| National Instruments | LabWindows/CVI |

* Specifications subject to change without notice.

Interface Technology, Inc. • 300 S. Lemon Creek Dr., • Walnut CA • 91789
Phone: (909)595-6030 • FAX: (909)595-7177 • e-mail: info@interfacetech.com • www.interfacetech.com

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