Agilent 83496B Clock Recovery Module With PLL Analysis

Increased eye-mask and jitter measurement accuracy with breakthrough performance in clock recovery circuitry

- **Continuous, unbanded tuning from 50 Mb/s to 14.2[1] Gb/s**
- **Ultra low residual jitter: < 300 femtoseconds rms**
- **Golden PLL operation with a tunable loop bandwidth from 30 kHz to 10 MHz for configurable industry standard compliant test**
- **High gain for tracking spread-spectrum signals**
- **PLL BW/jitter transfer and phase noise/jitter spectrum analysis**

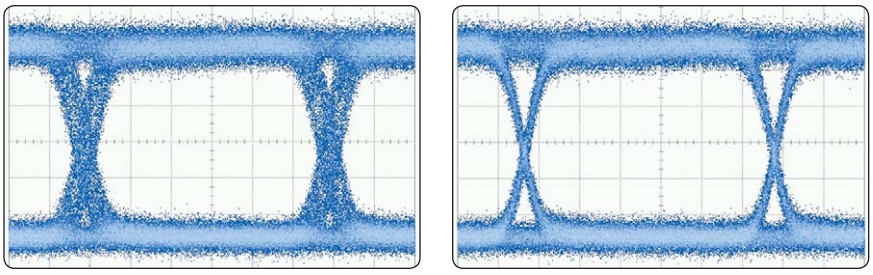
Wide-bandwidth sampling oscilloscopes provide essential information about high-speed digital communication transmission. When the necessary synchronous trigger is not available, a common solution is to derive a clock from the data being measured. But the recovered clock approach can be more than just an alternative method for instrument synchronization.

Many test standards (IEEE 802.3 Ethernet, Fibre Channel etc.) require the use of a "Golden PLL" (phase locked loop) jitter transfer characteristic or loop bandwidth to control what spectrum of jitter is observed and what is removed from eye-mask and jitter tests. If the loop bandwidth is too wide, too much high-frequency jitter is removed from the observed signal. If the loop bandwidth is too narrow, measurements can be obscured with lower frequency jitter. This jitter is usually less important since receivers easily tolerate this. Testing with an optimal loop bandwidth assures that good parts do not appear to be bad, and bad parts do not appear to be good.

The 83496B clock recovery module provides ideal performance for waveform analysis with the 86100 Digital Communications Analyzer. It can derive a clock from NRZ signals with rates as low as 50 Mb/s, as high as 14.2[1] Gb/s, and any rate between, providing the ultimate in flexibility and value. At under 300 femtoseconds rms, the residual jitter of the output clock is virtually negligible, allowing accurate measurements of very low levels of signal jitter.

A well-designed clock recovery circuit can significantly enhance the accuracy of eye-mask and jitter analysis. It can be a fundamental element of many jitter and eye-mask test strategies.

The 83496B has a tunable loop bandwidth. This critical feature allows the module to be configured as a Golden PLL with the optimal loop bandwidth for whatever standard/data rate is being tested. Test systems can now be designed according to the exact specifications of industry standards. Measurement precision is enhanced and test margins can be significantly increased



Observed jitter can be significantly reduced through a compliant clock recovery circuit

[1] Requires 86100C firmware revision 8.1

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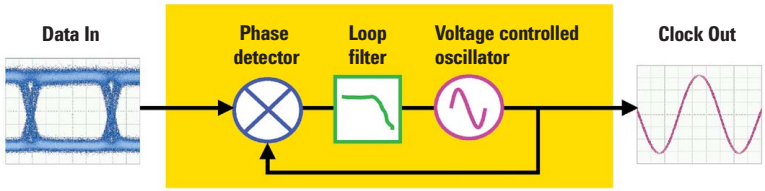
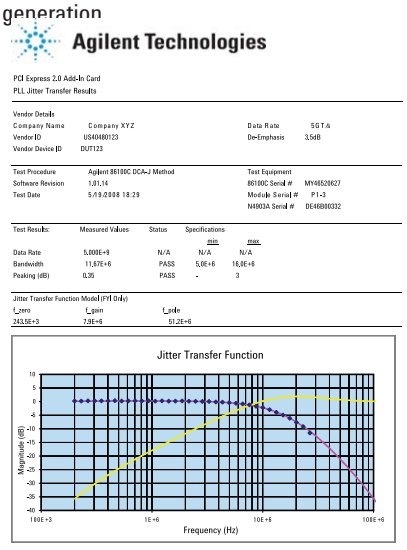
83496B block diagram



Using hardware from Agilent precision signal sources and patented technology from Agilent Laboratories, the 83496B raises clock recovery performance from "off-the-shelf" to a high-quality instrumentation grade level. The 83496B is available in either of two configurations: Option 100 for electrical applications and Option 101 for optical and electrical applications.

PLL and jitter spectrum analysis

Use 86100CU-400 software to make fast, accurate and repeatable measurements of phase-locked loop (PLL) bandwidth/jitter transfer. With a precision jitter source, the 83496B can be configured as a jitter receiver to create a PLL stimulus-response test system. PCI Express® approved PLL bandwidth compliance tests and SONET/SDH jitter transfer measurements are pre-configured, with automatic report generation.



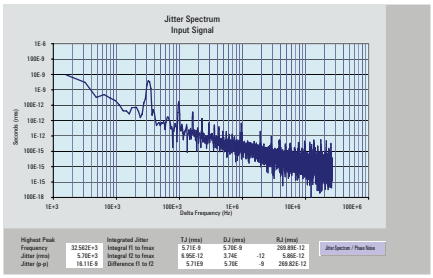
Built-in PLL bandwidth compliance reports

See 86100CU-400 PLL and jitter spectrum measurement software, publication number 5989-9319EN and Product Note 86100C-2, "Understanding Jitter Through Phase Noise Analysis", literature number 5989-6551EN.

Operating range:	50 Mb/s to 7.1 Gb/s
With Option 200:	50 Mb/s to 14.2 Gb/s
Residual jitter (jitter free input):	< 300 fs rms[1]
Loop BW:	270 kHz or 1.5 MHz
With Option 300:	15 kHz to 10 MHz[1] or fixed ratio of data rate/N
Wavelength range: (Option 101)	780 to 1330 nm MMF (62.5 um) 1250 to 1620 nm SMF (9 um)

83496B is only compatible with the 86100C mainframe.

86100CU-400 software and the 83496B also provide insights into the root causes of jitter through phase noise and jitter spectrum analysis on both clock and data signals.



Phase noise/jitter spectrum plots reveal jitter sources

Option 100: Electrical differential or single-ended clock recovery 50 Mb/s to 7.1 Gb/s. The input signal is internally split and ~50% routed back out to the measurement channel of the adjacent plug-in module.

Option 101: Optical single-mode 1250 to 1620 nm and multimode 780 to 1330 nm clock recovery 50 Mb/s to 7.1 Gb/s. The input signal is internally split and 70% multimode or 50% single-mode is routed back out to the measurement channel of the adjacent plug-in module. The Option 101 configuration will also accept a differential or single-ended electrical signal, but the signal split or tap must be performed external to the module.

Option 200: Increase operating range to 14.2 Gb/s. Available for either Option 100 or Option 101 configurations.

Option 201: Operating range of either Option 100 or Option 101 is set to be 7.1 to 14.2 Gb/s (operation from 50 Mb/s to 7.1 Gb/s becomes unavailable).

Option 300: Add Golden PLL (tunable loop bandwidth capability). Loop bandwidth is tunable from 15 kHz to over 10 MHz. (Without Option 300, the loop bandwidth can be configured at 270 kHz or 1.5 MHz). Available for either Option 100 or 101 configurations.

The recovered clock signal is routed internally to the 86100 mainframe and is also available at the front panel. Above 7.1 Gb/s, the front panel recovered clock is a subrate clock. Option 200 and 300 can also be added after initial purchase by returning the module to an Agilent service center for the upgrade.

1 Specification varies with data rate

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Online Assistance:
www.agilent.com/find/83496B

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

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Product specifications and descriptions in this document subject to change without notice.

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