Agilent E4861B ParBERT 3.35 Gb/s Data Module
Agilent E4862B ParBERT 3.35 Gb/s Generator Front-End
Agilent E4863B ParBERT 3.35 Gb/s Analyzer Front-End

Technical Specifications

General

A ParBERT 3.35 Gb/s module can house up to two front-ends, either two generators or analyzers or any mix. ParBERT 3.35 Gb/s modules work with the E4808A or E4890A clock modules. The key specifications of ParBERT 3.35 Gb/s modules are:

- 21 MHz ... 3.350 GHz clock/data rate
- 16 Mbit memory depth at each channel
- HW-based PRBS generation up to the polynomial of $2^{31}-1$
- Analyzer can synchronize on a 48 bit detect word (memory-based data)
- Analyzer can synchronize on a pure PRBS pattern without detect word

Timing capabilities

The frequency range of the modules is 21 MHz ... 3.350 GHz. The ParBERT 3.35 Gb/s front-ends use a multiplying PLL that multiplies system master clock by 4 or 8. Through the clock module, an external clock source can be used. This external clock must run continuously. If the clock signal is interrupted, the multiplying PLLs typically needs 100 milliseconds to lock onto the clock again.

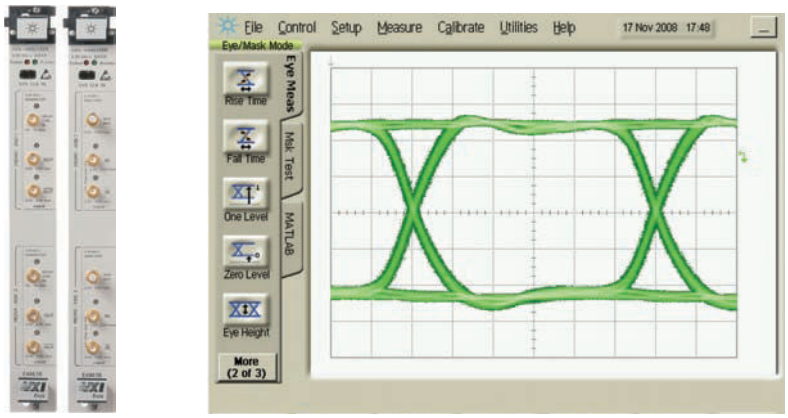

Figure 23. E4861B and E4862B with waveform of E4861B generator

Table 43. E4861B data generator timing specification (@ 50% of amplitude, 50 Ω to GND)

Frequency range	20.834 MHz to 3.350 GHz
Delay = start delay + fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 200 ns (not limited by period)
Fine delay range	±1 period (can be changed without stopping)
Delay resolution	1 ps
Accuracy data mode	±25 ps ±50 ppm relative to the zero-delay and temperature change within ±10 °C after autocalibration
Clock mode	±50 ps ±50 ppm relative to the zero-delay
Skew between modules of same type (data mode)	50 ps typ. after deskewing at customer levels and unchanged system frequency

The variable delay is available in data mode and pulse mode. In clock mode the timing is fixed.

Sequencing

The sequencer receives instructions from the clock module. The channel sequencer can generate a sequence with up to 60 segments. An analyzer channel can generate feedback signals which are combined in the clock module for a common response of all parallel channels. With a single receiver channel the channel sequencer itself handles the feedback signals.

Table 44. E4861B analyzer timing all timing parameters are measured at ECL levels, terminated with 50 Ω to GND

Sampling rate	20.834 MHz to 3.350 GHz
Sample delay	Same as delay = start delay + fine delay
	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 200 ns (not limited by period)
Fine delay range	±1 period (can be changed without stopping)
Resolution	1 ps
Accuracy	±25 ps ±50 ppm relative to the zero-delay and temperature change within ±10 °C after autocalibration
Skew	50 ps typ. after deskewing at customer levels and unchanged system frequency

Table 45. E4861B pattern and sequencing

Patterns	
Memory based	Up to 16 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
Analyzer auto-synchronization	On PRBS or memory-based data Manual or automatic by: Bit synchronization(1) with or without automatic phase alignment. Automatic delay alignment around a start sample delay (range: ± 10 ns) BER threshold: 10^{-4} to 10^{-9}

(1) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect word at the beginning of the segment, and the generators must be on a separate system clock. “Don’t cares” within detect word are possible. If several inputs synchromize, the delay diffference between terminals must be smaller than ±5 segment length resolution.

Table 46. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mb/s	Segment length	Maximum memory resolution depth, bits
20.834 ... 41.666	1 bit	131,072
20.834 ... 82.333	2 bits	262,144
20.834 ... 166.666	4 bits	524,288
20.834 ... 333.333	8 bits	1,048,576
20.834 ... 666.666	16 bits	2,097,152
20.834 ... 1,333.333	32 bits	4,194,304
20.834 ... 2,700.000	64 bits	8,388,608
20.834 ... 3,350.000	128 bits	16,777,216

Table 47. Dependancy of PRWS generation and port width.

Almost all the combinations are possible except the following:	
PRWS	Port width
2^7 - 1	No restriction
2^9- 1	7
2^{10}- 1	3, 11, 31, 33
2^{11}- 1	23
2^{15}- 1	7, 31
2^{23}- 1	47
2^{31}- 1	No restriction

Pattern generation

The data stream is composed of segments. A segment can be a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 16 Mbit (at segment length resolution 128 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15}- 1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio. A zero substitution pattern extends the longest zero series by a user-selectable number of additional zeros. The next bit following these zero-series will be forced to 1. Mark ratio is the ratio of ones and zeros in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4, 7/8. Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 128 the number of repetitions is also 128. That means that a 2^{15}- 1 PRBS uses up to 4 Mbit of the memory. Hardware-based PRBS can be any polynomial up to 2^{31}- 1. No memory is used, so the total memory is free for memory-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a ‘0’ a ‘1’ is generated and vice versa. Single errors can be inserted by pod or via instruction from the central sequencer. The user can trigger an error with a signal supplied to the qualifier pod of the central module. An error insertion with a fixed rate and a fixed distribution is supported. The user software allows the selection of errored and error-free segments.

Generator front end (E4862B)

The amplifier generates a differential output signal. Each output can be individually switched on and off. The output levels are sufficient to drive typical high-speed devices with interfaces like ECL, PECL, LVDS and DVI levels. The nominal output impedance is 50 Ω. The delay control has a single-ended input with 50 Ω impedance. The input voltage modulates a delay element within the generator's differential output. The user has the option of turning the delay control in feature on or off. Additionally the user can select between two delay ranges.

Table 48. Parameters for generator front-ends E4862B 3.35 Gb/s

Outputs	1, differential or single-ended	
Impedance	50 Ω typ.	
Data formats	Data: NRZ, DNRZ, RZ, R1	
Pulse mode Range Sampling delay resolution Width accuracy	 150 ps to (1UI - 150 ps) 1 ps 40 ps typ.	
Output voltage window	–2.00 to +3.5 V	(1)
Ext. term. voltage	–2.00 to +3.5 V	(2)
Absolute maximum external voltage	–2.2 V to +3.2 V	
Addressable technologies	LVDS, CML, PECL, ECL low voltage CMOS	
Amplitude/resolution	0.05 Vpp ... 1.8 Vpp/10 mV	
Accuracy hi level/amplitude	±2% ±10 mV	
Short circuit current	72 mA max.	
Transition times (20% - 80%)	< 75 ps; 60 ps typ.	
Overshoot/ringing	5% +10 mV typ.	
Jitter, NRZ data mode Clock mode Pulse, RZ, R1 mode	< 30 ps peak-peak < 2 ps rms 30ps peak-peak typ.	(3) (3 & 4) (3 & 4)
Cross-point adjustment (Duty cycle distortion)	30% ... 70% (in NRZ mode only)	

(1) For output voltages > 3 V the termination voltage ≥ 3 V needs to be applied.
(2) External termination voltage must be less than 3 V below VOH. and less than 3 V above VOL. Termination into AC is possible.
(3) Measured with E4808A clock module.
(4) Specified as intra channel jitter.

Table 49. Delay control in

Input voltage window	–500 mV to +500 mV (DC-coupled)
Delay range 1	–250 ps to +250 ps
Delay range 2	–25 ps to +25 ps
Modulation bandwidth	DC to 200 MHz
Input impedance	50 Ω (typ.)

Typical waveform pictures

Eye Plots

The 3.35 Gb/s generator output is designed for clean and fast output signals. It offers a swing of 50 mV to 1.8 V within the voltage window suited for testing LVDS, CML, (P)ECL and SSTL 0 - 3.3 V technologies.

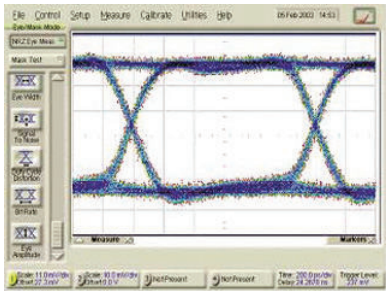

Figure 24a. 3.35 Gb/s Generator: 50 mVpp

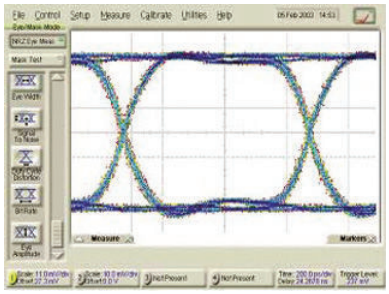

Figure 24b. 3.35 Gb/s Generator: 1.8 V pp

Crossing Point

The 3.35 Gb/s generator allows a variable cross-over for differential signals. The cross-over can be programmed by the user interface or remote program between 30 and 70%.

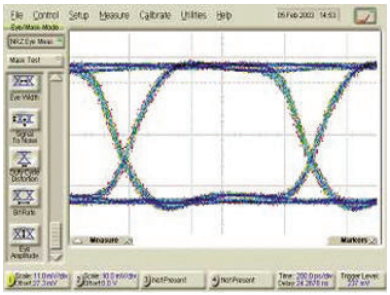

Figure 24c. 3.35 Gb/s Generator @30%

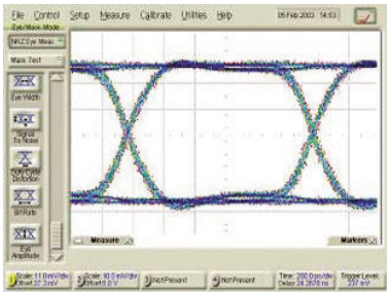

Figure 24d. 3.35 Gb/s Generator @50%

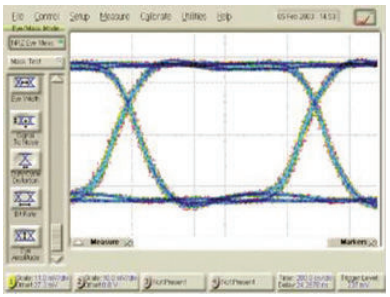

Figure 24e. 3.35 Gb/s Generator @70%

Jitter Modulation Examples

A Receiver's jitter tolerance can be tested applying a voltage at the external delay control input and by this generating jittered output signals as depicted in figure 26 a-d.

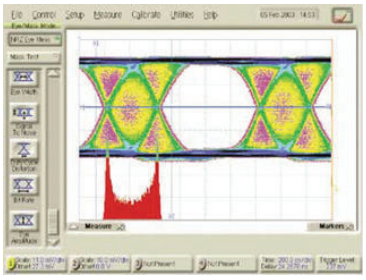

Figure 25a. Jitter modulated with sine wave

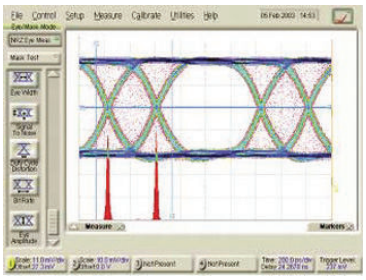

Figure 25b. Jitter modulated with rectangle wave

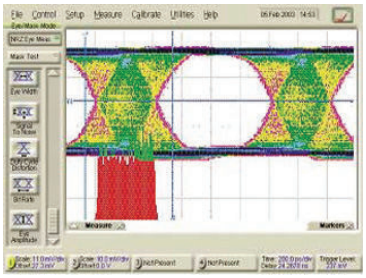

Figure 25c. Jitter modulated with triangle wave

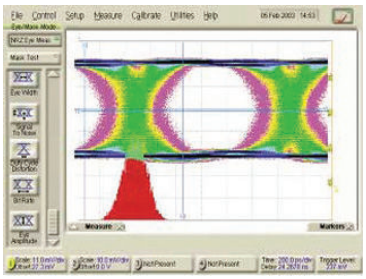

Figure 25d. Jitter modulated with noise generator

Analyzer front end (E4863B)

The analyzer features are:

- Acquire data from start
- Compare and acquire data around error
- Compare and count erro neous ones and zeros to calculate the bit error rate

The receive memory for acquired data is up to 16 Mbit deep, depending on the segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum granularity.

The analyzer is able to synchronize on a received data stream by means of a user-defined detect word. The detect word is defined by the first bits within the expected segment, it has a length of 48 bits and is composed of zeros, ones and Xs (“don’t cares”). The detect word must be unique within the data stream. Synchronization on a pure-PRBS data-stream is done without a detect-word, by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity is down to 50 mV and the common mode range of the comparator allows the testing of all common differential high-speed devices.The user has the option of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

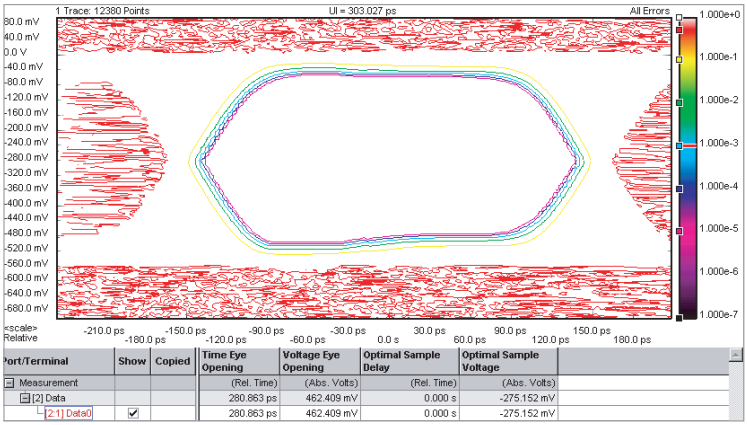

Figure 26. Eye diagram of E4863B analyzer

Table 50. Parameters for analyzer front-ends E4863B 3.35 Gb/s

Number of channels	1, differential or single-ended	
Impedance	50 Ω typ. (100 Ω differential if termination voltage is switched off)	
Internal termination voltage (can be switched off)	-2.0 to +3.0 V	
Threshold voltage range	-2.0 to +3.0 V	
Threshold resolution	1 mV	
Threshold accuracy	±20 mV ±1%	
Input sensitivity (single-ended and differential)	< 50 mV	
Minimum detectable pulse width	< 150 ps	
Maximum input voltage range	Three ranges selectable: -2 V to +1 V -1 V to +2 V 0 V to 3 V	
Maximum differential voltage	1.8 V	
Phase margin with ideal input signal	> 1 UI - 30 ps	(1)
Phase margin with E4862B generator	> 1 UI - 50 ps	(1)
Auxilary out	V out: 350 mV pp typ., AC coupled	(2)
Sampling delay resolution	1 ps	

(1) Measured with E4808A central module

(2) Terminate with 50 Ω to GND, if not used

Protection

Input and output relays switch off automatically, if the absolute maximum voltage window is exceeded.