Agilent U4154A

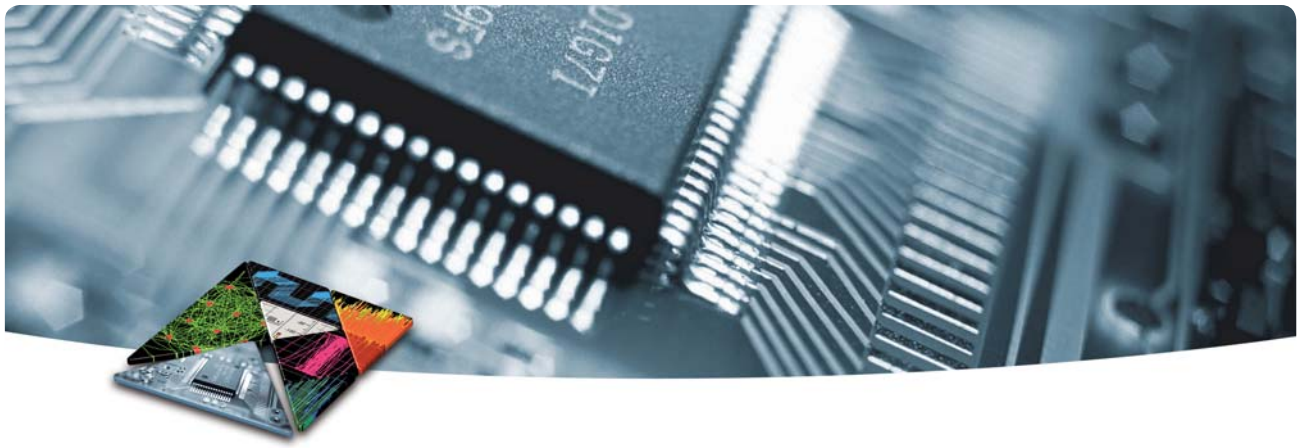
4 Gb/s AXIe-based
Logic Analyzer Module

Data Sheet

DISCOVER the Alternatives...

... Agilent **MODULAR** Products

Agilent Technologies



INTRODUCTION

Product Description

The Agilent U4154A AXIe-based logic analyzer system combines reliable data capture with powerful analysis and validation tools to enable you to quickly and confidently validate and debug high speed digital designs operating at speeds up to 4 Gb/s.

Figure 1A shows the small eyes associated with a DDR3 system operating at 1.4V at a frequency of 2066 Mb/s. The U4154A logic analyzer uses its unique eye scan capability to automatically place the sampling point in both time and voltage within the eye on each individual channel for optimal sampling reliability.

Figure 1B shows the trigger setup to capture a burst of 8 Writes. The trigger sequencer operates up to 2.5 Gb/s, enabling accurate and precise triggering.

Figure 1 C and D show the state listing and waveform for this capture.

12.5 GHz Timing Zoom with 256K sample memory gives you simultaneous state and high-resolution timing measurements covering a time span of 20 us, which corresponds to 43680 clock cycles at a 2133 MHz clock rate.

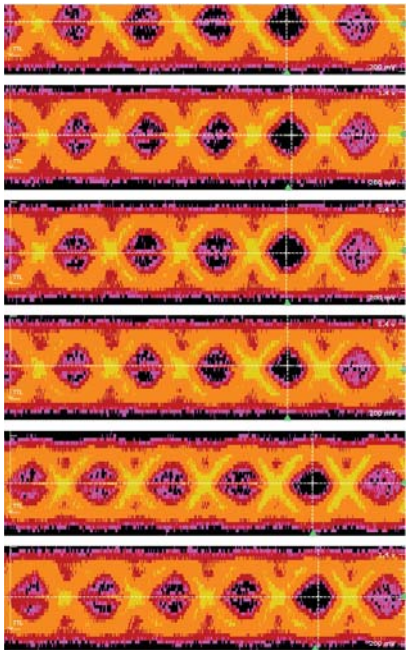


Figure 1A

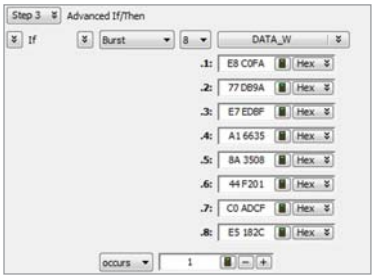


Figure 1B

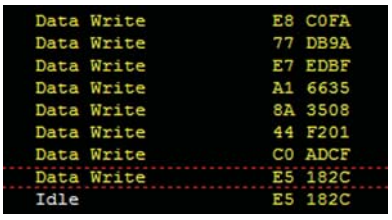


Figure 1C

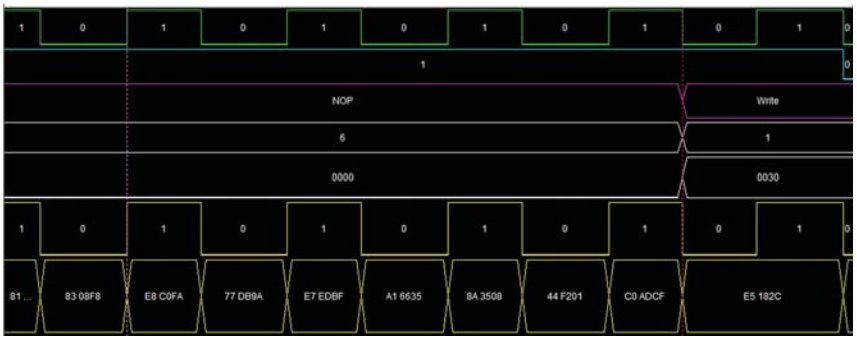


Figure 1D

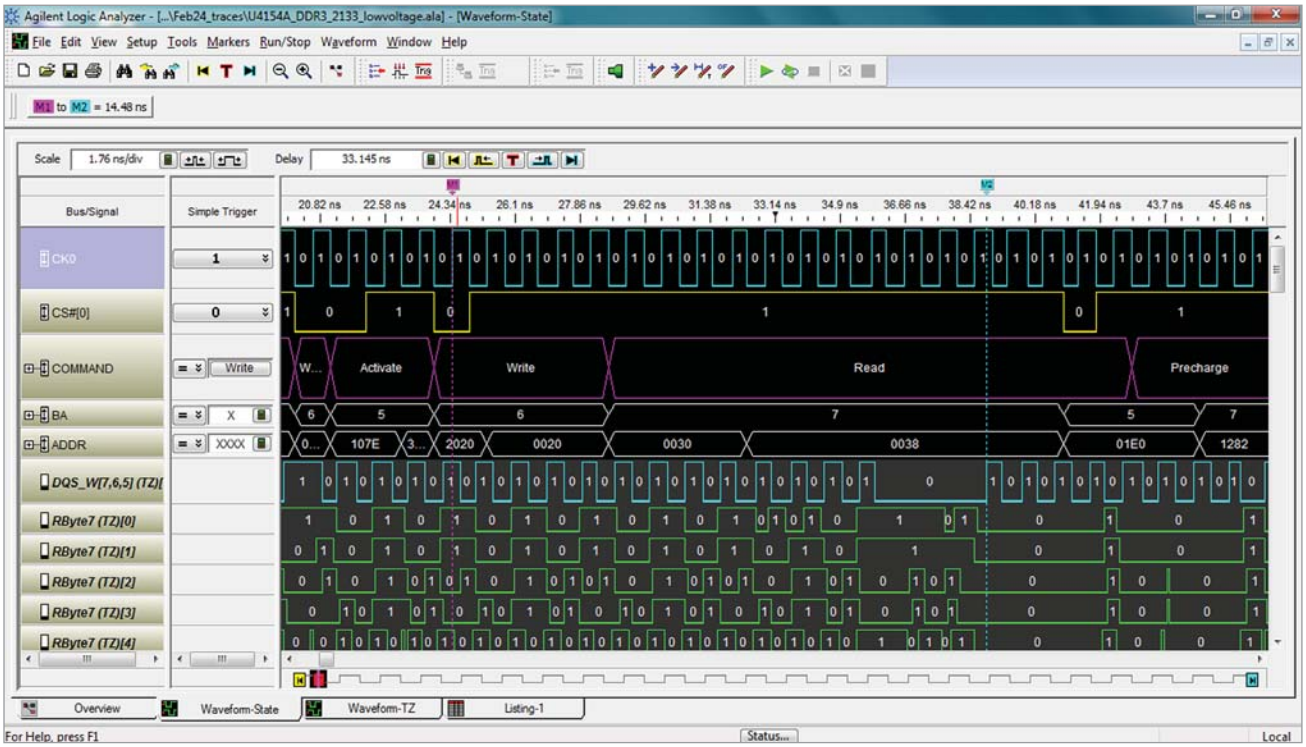


Figure 2. Timing Zoom precisely measures the time between the rising edge of the clock and the rising edge of DQS in a DDR system.

Available memory depth up to 200 M samples allows you to debug very complex problems where the cause and symptoms may be separated by several seconds. The amount of memory can upgraded after purchase; see "Upgrades" in "Ordering Information."

No need to sacrifice sampling resolution to view more system activity. In timing mode, if your system has bursts of activity followed by times with little activity, you can use transitional timing along with the logic analyzer's deep memory to capture seconds to minutes of activity at 400 ps (2.5 GHz) sampling resolution. You also have the flexibility to increase the amount of time captured by excluding certain buses or signals from being stored, for example clock or strobe signals that add little useful information to the measurement. In State mode, use store qualification to save only states of interest into memory.

The dual-sample mode has two benefits: For DDR memory signals, it will separate reads from writes, with automatic setup of the correct sampling positions for each. This mode also allows acquisition of state (synchronous) data at rates up to 4Gb/s. When used in this mode for non-DDR-memory signals, the data will appear in two labels. The labels can be merged using the Agilent B4602A Signal Extractor tool. When used to acquire DDR memory signals, the B4621A DDR or B4623A LPDDR2 decoders automatically merge the signals into one label. When operated in dual-sample mode on all pods, the channel count is 68 channels for one U4154A, or 136 channels for two U4154As combined. Dual-sample mode can be selected on a per-pod-pair basis, so if you have only a subset of signals that require dual-sample mode, the channel count can be higher.

Support for bursty clock allows you to take measurements that include periods of inactivity on the clock, such as power management transitions when the clock is inactive.

DDR measurements made fast, easy, and powerful

The DDR setup assistant simplifies measurement setup and minimizes the time to make your first measurement. The DDR setup tool guides you through even the most complex DDR setup in minutes. DDR eye scan makes it easy to determine the optimum acquisition sample point without requiring an oscilloscope. Agilent qualified scans place the sample position at the center of the eye on every individual channel for maximum data capture reliability, including separate sampling positions for read and write data. The DDR setup assistant includes a variety of powerful, time-saving trigger features optimized for DDR measurements. Burst trigger captures an entire data burst of 8 on DDR2/3 systems from one sequence level in the trigger menu. Intuitive trigger macros with diagrams provide visualization of triggering options and simplify the process of creating triggers.

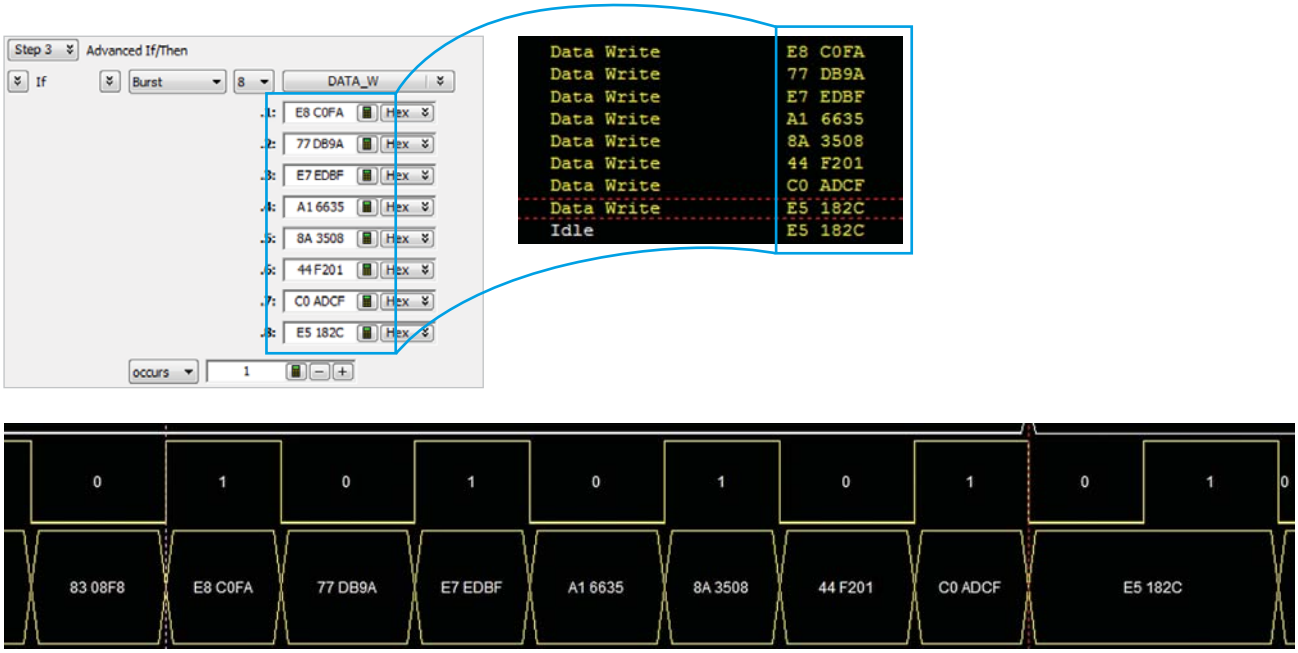


Figure 3 Burst recognizer trigger makes it easy to trigger on events in a burst read or write

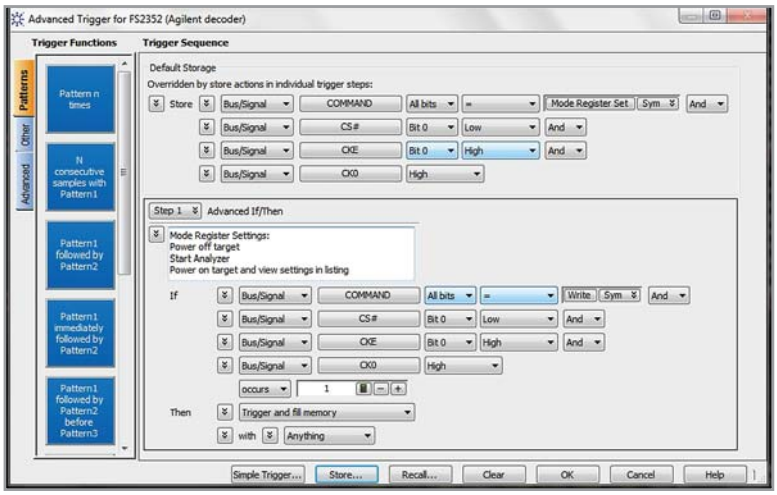


Figure 4 Mode register set trigger allows you to capture key events during initialization without wasting valuable memory

Signal Integrity Insight Made Fast and Easy

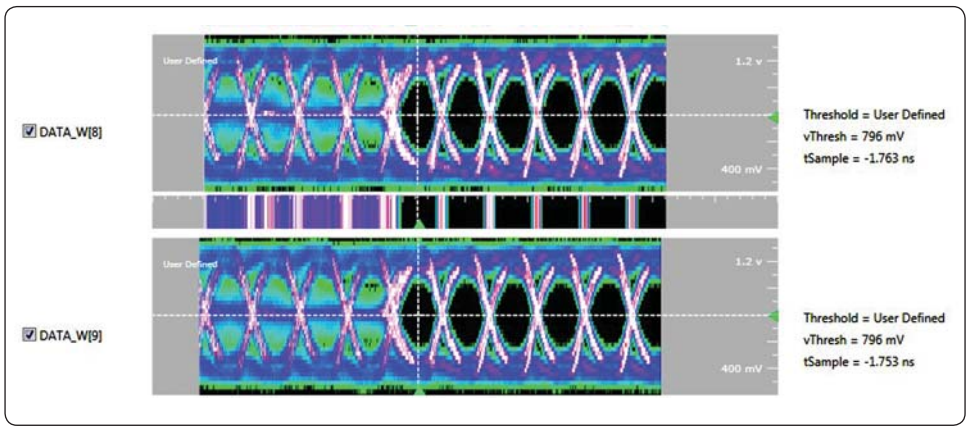


Figure 5. Burst qualified eye scan allows you to view the activity on the signals only when a burst it taking place.

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes. Identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses. Support for up to 4 clock qualifiers, the ability to qualify scans of any signal from any combination of other signals, full triggering capabilities for scan qualification, and customizable viewing windows allows you to sample only when the qualifying signal is active and see specific system activity of interest. The eye scan technology in the U4154A provides insights that can't be achieved with any other test method.

DDR eye scan automatically groups signals so you can quickly spot byte lane related signal integrity problems. Scans can be qualified based on state trigger criteria, thus providing unique insight. For example, read and write scans can be separated for greater insight. Burst scan allows you to gather signal integrity information on two read or write cycles separated by only one cycle.

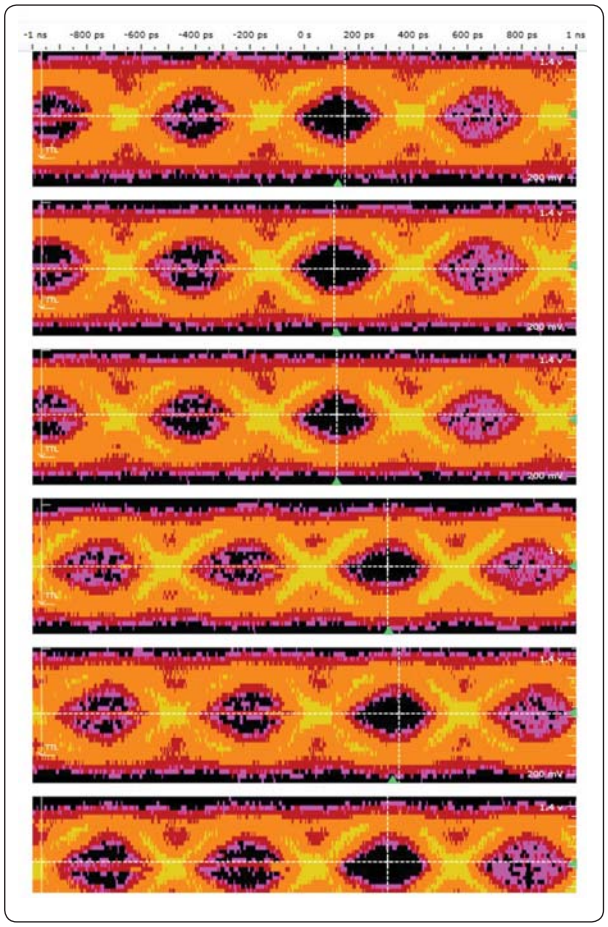


Figure 6. Eye scan clearly indicates the byte lane shift caused by fly-by routing.

Harness Your Logic Analyzer and Scope for Powerful Insight

Combine the powerful triggering and protocol analysis of a logic analyzer with the signal integrity insight of a scope to solve tough design problems. Agilent ViewScope allows you to easily make time-correlated measurements between Agilent logic analyzers and oscilloscopes. The time-correlated logic analyzer and oscilloscope waveforms are integrated into a single logic analyzer waveform display for easy viewing and analysis. You can also trigger the oscilloscope from the logic analyzer (or vice versa), and automatically de-skew the two instruments.

ViewScope enables you to perform the following tasks more easily, quickly, and effectively:

- Validate signal integrity
- Track down problems caused by signal integrity
- Validate correct operation of A/D and D/A converters
- Validate correct logical and timing relationships between the analog and digital portions of a design

Operating modes

Operating mode	Conventional state (synchronous)	Dual sample state	Conventional timing full channel	Conventional timing half channel	Transitional timing	TimingZoom
Acquisition rate	2.5 Gb/s	4 Gb/s	2.5 GHz	5 GHz	2.5 GHz	12.5 GHz
Number of channels in one U4154A	136	68	136	68	136	136
Number of channels in two U4154As combined	272	136	272	136	272	272
Memory depth (samples)						
Opt 002 (std)	2M	4M	2M	4M	2M	256K
Opt 004	4M	8M	4M	8M	4M	256K
Opt 008	8M	16M	8M	16M	8M	256K
Opt 016	16M	32M	16M	32M	16M	256K
Opt 032	32M	64M	32M	64M	32M	256K
Opt 064	64M	128M	64M	128M	64M	256K
Opt 128	128M	256M	128M	256M	128M	256K
Opt 200	200M	400M	200M	400M	200M	256K

Contact Agilent Technologies for information on additional configurations.

Note: Memory can upgraded after purchase. See “Upgrades” in “Ordering Information.”

When You Need More Channels or More Functions

Multiframe allows you to combine any combination of M9502A chassis and Agilent 16902B frames up to a total of 16 frames plus chassis.

Refer to **www.agilent.com/find/logic_modules** for information on modules available for the 16900 system.

Note: One PC host is required for each M9502A chassis.

Applications

- Functional and parametric validation of DDR3/4 memory systems and other high-speed digital systems operating up to 4 Gb/s
- Debug of hardware and software in high-speed digital systems operating up to 4Gb/s DDR3/4 memory systems.

Features

- State capture up to 4 Gb/s on 68 channels, 2.5 Gb/s on 136 channels per module
- Reliable data capture on eye openings as small as 100 ps by 100 mV
- 12.5 GHz Timing Zoom with 256 K sample memory
- Memory depth up to 200M samples
- Wide variety of probing solutions including BGA, interposer, mid-bus, and flying leads
- Up to 10,880 channels in a system using Multiframe

Customer values

- Confidence in state measurements with signal eye openings as small as 100 ps by 100 mV
- Rapidly view signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes.
- Quickly and easily set up complex DDR measurements

Hardware platform

Minimum Hardware

One or more U4154A 136-channel logic analyzer modules. Two U4154As can be combined for a total of 272 channels on a single time base and trigger sequencer. Two U4154As are required to capture all read and write data on a 64 Data bit DDR2/3 memory interface. DDR solutions requiring 5 pods or less require one U4154A module.

One Agilent M9502A 2-slot AXie chassis.
Refer to **www.agilent.com/find/axie-chassis**

One user-supplied PC equipped with Microsoft Windows® XP (32-bit), Microsoft Windows® Vista (32/64-bit), or Microsoft Windows® 7 (32/64-bit), and PCIe link or capable of accepting a PCIe adapter.

For laptop PCs:

One Agilent M9045A PCIe ExpressCard Adaptor

One Agilent Y1200A PCIe cable: x4 to x8, 2.0m

For desktop PCs:

One M9047A PCIe Desktop Adaptor

One Y1202A PCIe cable: x8, 2.0m

As many U4201A logic analyzer probe cables as required to connect the desired number of probes. One cable is required for every 34 channels.

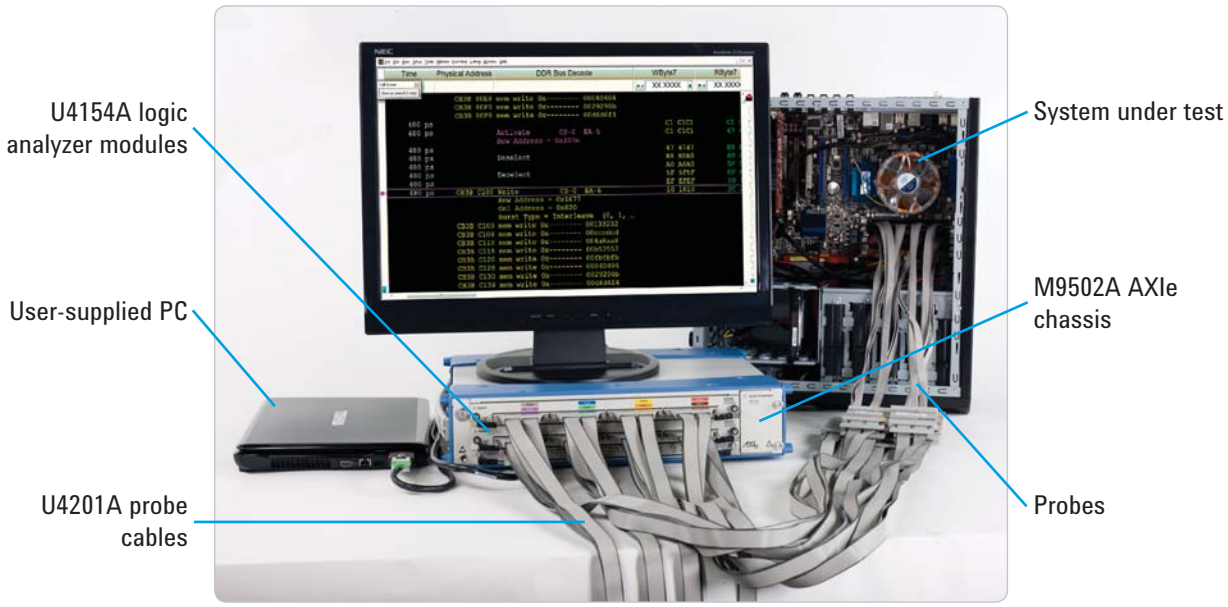


Figure 7. System components

Probes as required to connect to the target system.

Probe type	Model number	Channels	Maximum data rate	Supported signal types
Soft touch Connectorless Pro series	E5406A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft touch Connectorless Low profile	E5402A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft touch Connectorless Classic	E5390A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft touch Connectorless Half-size	E5398A	17 (16 data, 1 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft touch Connectorless Pro series	E5405A	17 (16 data, 1 clock)	4 Gb/s	Differential or single-ended data, differential or single-ended clock
Soft touch Connectorless Classic	E5387A	17 (16 data, 1 clock)	4 Gb/s	Differential or single-ended data, differential or single-ended clock
Samtec connector	E5378A	34 (32 data, 2 clock)	1.5 Gb/s	Single-ended data, Differential or single-ended clock
Samtec connector	E5379A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, Differential or single-ended clock
Mictor connector	E5380A	34 (32 data, 2 clock)	600 Mb/s	Single-ended data, Differential or single-ended clock
General purpose flying leads	E5382A	17 (16 data, 1 clock)	1.5 Gb/s	Single-ended data, Differential or single-ended clock
General purpose flying leads	E5381A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, Differential or single-ended clock

Recommended probes for DDR3 include BGA probes, interposers, and Soft Touch mid-bus probes. Interposers are available from FuturePlus Systems and Nexus Technology. Refer to “Ordering Information.”

Optional Hardware

Multiframe extensions

Additional M9502A chassis, or one or more Agilent 16902B logic analyzer frames with any of the modules that are compatible with the 16900 system. Refer to **www.agilent.com/find/16900** and to the *16900 Series Logic Analysis System Mainframes Data Sheet*. Up to 16 M9502A or 16902B frames can be combined in a single Multiframe system.

One or more E5861A Multiframe cables to connect multiple frames. Order one fewer E5861A cables than the total number of frames/chassis to be combined.

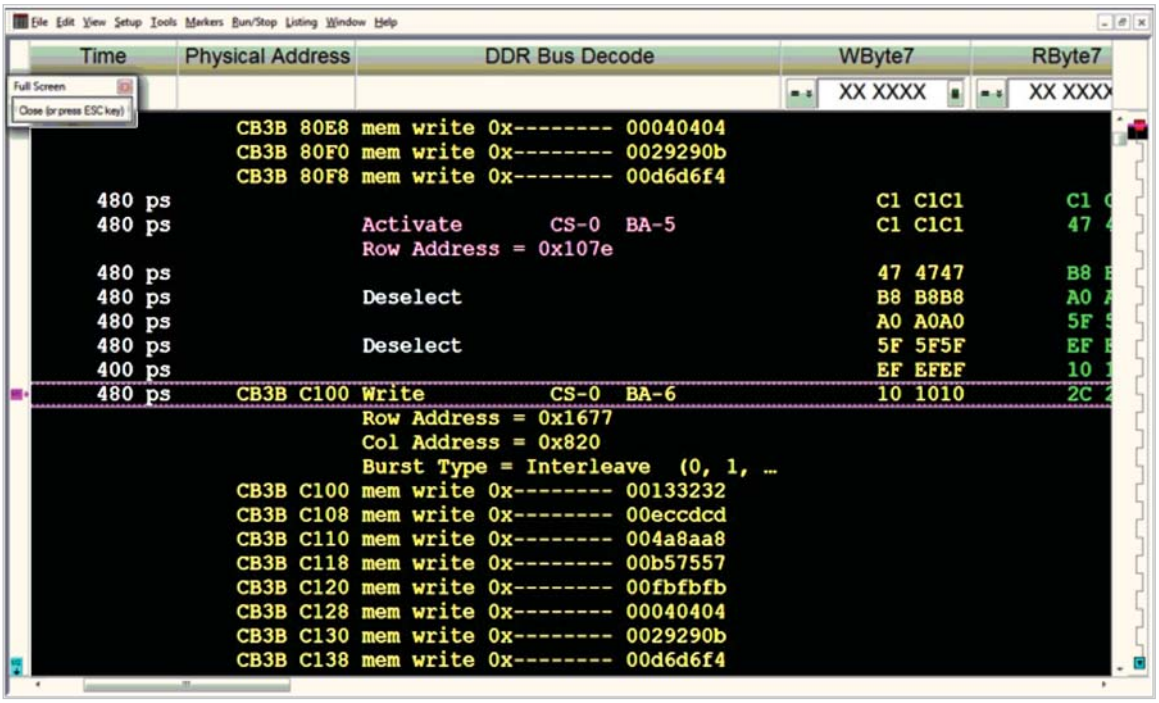


Figure 8. The B4621A protocol-decode software displays acquired signals as easily understood bus transactions

Optional Software

B4622A DDR2/3 Protocol Compliance and Analysis Tool

The Agilent B4622A DDR2/3 protocol compliance and analysis tool enables automated measurements on deep DDR bus traces to quickly identify protocol problem areas and provides an overview of system performance. In addition you can quickly setup physical address triggers with the DDR trigger tool. Up to three types of protocol violations and twelve types of protocol timing violations can be checked simultaneously. Performance analysis includes bus statistical information, in addition to a histogram view of the number of accesses at a specific memory address.

Bus Decoders for DDR2 and DDR3 Validation

The B4621A bus decoder for DDR2 and DDR3 and B4623A for LPDDR2 and LPDDR3 validation provide complete protocol decode of memory transactions using an Agilent logic analyzer as the analysis execution engine. The B4621A protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed.

The B4623A bus decoder for LPDDR and LPDDR2 validation provides complete protocol decode of memory transactions using an Agilent logic analyzer as the analysis execution engine. The B4623A protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed.

For additional analysis software, refer to **www.agilent.com/find/logic-sw-apps**

Technical Specifications

All specifications refer to the combination of a U4154A Logic Analyzer Module, U4201A logic analyzer probe cable, and any Agilent Soft Touch probe

State (Synchronous) Sampling Mode	
Maximum state data rate	2.5 Gb/s on 136 channels per U4154A, using either or both edges of clock 4 Gb/s on 68 channels per U4154A, using both edges of clock
Maximum state clock frequency (typ)	2.5 GHz
Minimum state clock frequency [1] (typ)	12.5 MHz (single edge) 6.25 MHz (both edges)
Sample position adjustment resolution (typ)	5 ps
Sample position adjustment accuracy (typ)	± 150 ps
Minimum data valid window (typ)	100 ps
Minimum setup time (typ)	50 ps
Minimum hold time (typ)	50 ps
Minimum eye height (typ)	100 mV
Sample position adjustment range (typ)	7ns
Minimum state clock pulse width (typ)	200 ps
Number of clocks (nom)	1
Minimum time between active clock edges (typ)	400 ps
Maximum time between active clock edges [1] (typ)	80 ns
Number of clock qualifiers (nom)	4
Clock qualifier setup time (typ)	100 ps
Clock qualifier hold time (typ)	100 ps
Time tag resolution (typ)	80 ps
Maximum time count between stored states (typ)	66 days

1. Clock can pause for up to 66 days once every 8 or more edges

Timing (Asynchronous) Sampling Mode	Half-Channel mode	Full-Channel Mode
Maximum sample rate (nom)	5 GHz	2.5 GHz
Minimum sample period (nom)	200 ps	400 ps
Number of channels (nom)		
One U4154A	68	136
Two U4154A	136	272
Pod usage (nom)	1 pod from each odd/even pod pair, user selectable	All pods
TimingZoom sampling rate (nom)	12.5 GHz	
TimingZoom memory depth (nom)	256 Ksamples	
Maximum time between transitions (nom)	66 days	
Minimum data pulse width (typ)	1 sample period + 200 ps	
Time interval accuracy (typ)	± (1 sample period + 400 ps + 0.01% of time interval reading)	

Trigger Characteristics	
Maximum trigger sequence speed (typ)	2500 MHz (400 ps)
Trigger resources (nom)	16 patterns evaluated as =, !=, >, >=, <, <= 8 double-bounded ranges evaluated as in range, not in range 4 to 8 burst detectors 4 edge detectors in timing, 3 in transitional timing 1 occurrence counter per sequence level 1 timer 3 flags 1 arm in
Trigger resource Boolean conditions (nom)	Arbitrary Boolean combinations
Trigger actions (nom)	Goto Trigger and fill memory Trigger and Goto Trigger, send e-mail, and fill memory
Store qualification actions (nom)	Default (global) and per sequence level Store/don't store sample Turn on/off default storing
Timer actions	Start from reset Stop and reset Pause Resume

Flag Actions	Set Clear Pulse set Pulse clear
Maximum trigger sequence levels (nom)	8
Trigger sequence level branching (nom)	Arbitrary 4-way if/then/else
Trigger position (nom)	Start, center, end, or user-defined
Maximum occurrence counter (nom)	999,999,999
Maximum pattern width (nom)	128 bits – single label 272 bits – AND of multiple labels across two-card set
Maximum range width (nom)	64 bits
Timer range (nom)	100 ns to 27 hours (in timing modes) 200 * state clock period to 27 hours (in state mode)
Timer resolution (nom)	5 ns
Timer accuracy (typ)	± (5 ns +0.01%) (in timing modes) ± (8 * state clock period +2ns +0.01%) (in state mode)
Timer reset latency (nom)	40 ns (in timing modes) 80 * state clock period (in state mode)

Definitions for Specifications

General	
Number of channels (nom)	136 in one U4154A 272 in two U4154As combined
Maximum channels on a single time base and trigger (nom)	272
Number of analyzers (nom)	1
Input signal amplitude V_{amptd} (typ)	=>350 mV
Supported signal types	Single-ended and differential
Voltage threshold (typ)	-5V to +5V
Threshold resolution (typ)	2 mV
Threshold accuracy (typ)	±(30 mV + 1% of setting)
Threshold setting granularity	By channel

Environmental and Physical

Operating environment	
Temperature (nom)	0 deg C to +40° C
Humidity (nom)	0 to 80% relative humidity at 40° C
Altitude	0 to 3000 m
Vibration	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms

Non-operating environment	
Temperature (nom)	–40° C to +75° C
Humidity (nom)	0 to 90% relative humidity at 65° C
Altitude	0 to 15,300 m
Vibration (in shipping carton)	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Weight	
Weight	2.34 kG

Specification (spec): Represents warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 to 40° C, unless otherwise stated, and after a 45 minute warm-up period. The specifications include measurement uncertainty. Data represented in this document are specifications unless otherwise noted.

Typical (typ): Represents characteristic performance, which 80% of the instruments manufactured will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 25° C).

Nominal (nom): The expected mean or average performance, or an attribute whose performance is by design, such as the 50 Ω connector. This data is not warranted and is measured at room temperature (approximately 25° C).

Measured (meas): An attribute measured during the design phase for purposes of communicating expected performance, such as amplitude drift vs. time. This data is not warranted and is measured at room temperature (approximately 25° C).

Configuration

Recommended configuration for DDR2/3 analysis		
Model	Quantity	Description
U4154A Option 02G	2	Logic Analyzer, 136-channel, 12.5 GHz timing zoom, 2.5 GHz state, 2 Mb depth
M9502A	1	AXIe 2 slot chassis
U4201A	8	logic analyzer probe cable
M9045A or M9047A	1	PCIe ExpressCard Adaptor for laptops PCIe Desktop Adaptor
Y1200A or Y1202A	1	PCIe cable: x4 to x8, 2.0m,for use with M9045A PCIe cable: x8, 2.0mfor use with M9047A
Probes		As required, refer to ordering information. 8 probes are required to acquire all DDR2/3 signals.

Related products	
Model	Description
U4301A	PCIe Analyzer
FuturePlus FS2400 DDR3 Detective	DDR3 Detective™ For Use With Agilent Logic Analyzers and Oscilloscopes

Ordering

Model	Description
U4154A Option 02G	Logic Analyzer, 136-channel, 12.5 GHz timing zoom, 2.5 GHz state, 2 Mb depth
Option 002	2M sample memory depth (standard)
Option 004	4M sample memory depth
Option 008	8M sample memory depth
Option 016	16M sample memory depth
Option 032	32M sample memory depth
Option 064	64M sample memory depth
Option 128	128M sample memory depth
Option 200	200M sample memory depth
M9502A	AXIe 2 slot chassis
U4201A	Logic Analyzer Cable For Use With Individual Probes
E5861A	Multiframe Cable

Ordering (continued)

Probes	
Model	Description
W3631A	DDR3 x16 BGA Command and Data Probe for Logic Analyzer and Scope
W3633A	DDR3 x4/x8 BGA Command and Data Probe for Logic Analyzer and Scope
E5847A	46-ch Single-ended ZIF probe for DDR3 x4/x8 DRAM BGA probe connection to 90-pin logic analyzer cable
E5845A	46-ch Single-ended ZIF probe for DDR3 x16 DRAM BGA probe connection to 90-pin logic analyzer cable
E5406A	Pro Series Soft Touch Connectorless Probe - Single-ended, for 90-pin Cable (34 channels)
E5405A	Pro Series Soft Touch Connectorless Probe - Differential, for 90-pin Cable (17 channels)
E5402A	Low Profile, Pro Series Soft Touch Connectorless Probe - Single-ended, for 90-pin Cable
E5390A	Soft Touch Connectorless Probe-Single-ended, with 90-pin Cable Connectors
E5398A	Half-Size Soft Touch Connectorless Probe with 90-pin Cable Connectors
E5387A	Soft Touch Connectorless Probe-Differential, with 90-pin Cable Connectors
E5381A	Differential Flying Leads, 17 Channels
E5382A	Single-ended Flying Leads, 17 Channels
E5378A	Samtec Probe-Single-ended, with 90-pin Cable Connectors
E5379A	Samtec Probe-Differential, with 90-pin Cable Connectors
E5380A	Mictor Probe-Single-ended, with 90-pin Cable Connectors
Nexus Technology NT-DDR3DIHS	DDR3 1867 DIMM memory bus interposer
FuturePlus FS2352	DDR3 1867 DIMM interposer

DDR analysis software	
Model	Description
B4621A	Bus Decoder for DDR2 and DDR3 Validation
B4622A	DDR2/3 Protocol Compliance and Analysis Tool

Other software	
Model	Description
B4602A	Signal Extractor Tool
B4655A	FPGA dynamic probe for Xilinx
B4656A	FPGA dynamic probe for Altera
B4601C	Serial-to-parallel analysis package
B4606A	Advanced customization environment – development and runtime package
B4607A	advanced customization environment – runtime package
B4608A	ASCII remote programming interface
ASCII remote programming interface	Data import package
B4630A	MATLAB® connectivity and analysis package

Upgrades	
U4154U option 004	Upgrade memory to 4M
U4154U option 008	Upgrade memory to 8M
U4154U option 016	Upgrade memory to 16M
U4154U option 032	Upgrade memory to 32M
U4154U option 064	Upgrade memory to 64M
U4154U option 128	Upgrade memory to 128M
U4154U option 200	Upgrade memory to 200M

Warranty and Calibration

Advantage services: calibration and warranty

Agilent Advantage Services is committed to your success throughout your equipment's lifetime.

Calibration	Description
R1282A R-50C-011-3	Agilent Calibration - 3 years
R1282A R-50C-011-5	Agilent Calibration - 5 years
R1282A R-50C-021-3	ANSI Z540-1-1994 Calibration - 3 years
R1282A R-50C-021-5	ANSI Z540-1-1994 Calibration - 5 years

Warranty	Description
Standard warranty is 1 year	
R1280A R-51B-001-3C	Return to Agilent Warranty - 3 years
R1280A R-51B-001-5C	Return to Agilent Warranty - 5 years

The Modular Tangram

The four-sided geometric symbol that appears throughout this document is called a tangram. This seven-piece puzzle originated in China a few centuries ago. The goal is to create shapes—from simple to complex—that form an identifiable silhouette. As with a tangram, the possibilities may seem infinite as you begin to create a new test system. With a set of clearly defined elements—architecture, hardware, software—Agilent can help you create the system you need, from simple to complex.

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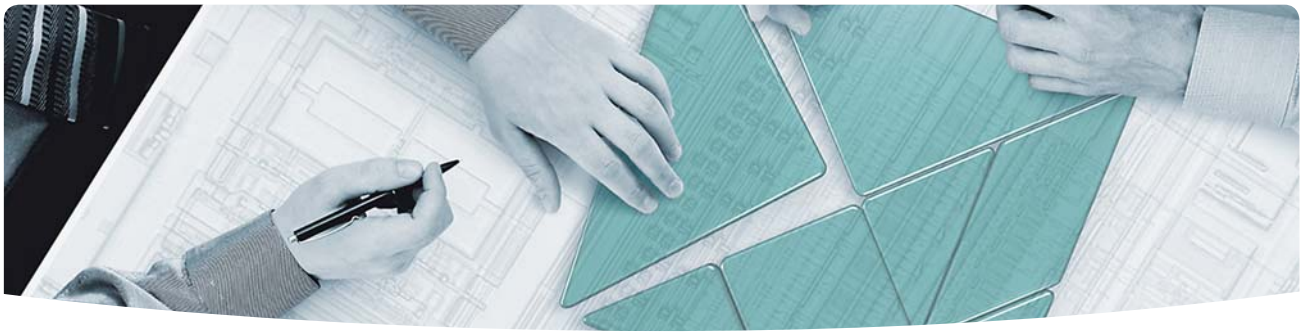

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