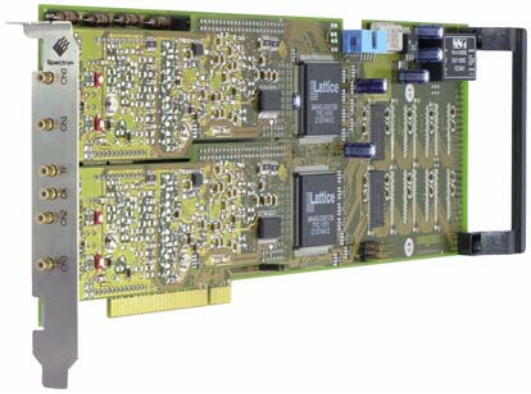
SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MI.30xx - 12 bit transient recorder up to 200 MS/s

- **Standard PCI format**
- **Fastest 12 bit A/D converter board**
- **Up to 200 MS/s on one channel**
- **Up to 100 MS/s on two channels**
- **Up to 60 MS/s on four channels**
- **Simultaneously sampling on all channels**
- **6 input ranges: ±200 mV up to ± 10 V**
- **Up to 256 MSample memory**
- **FIFO mode for slower samplerates**
- **Window and pulsewidth trigger**
- **Input offset up to ±100%**
- **Synchronization possible**



Product range overview

All 16 boards of the MI.30xx series may use the on-board memory completely for the currently active number of channels.

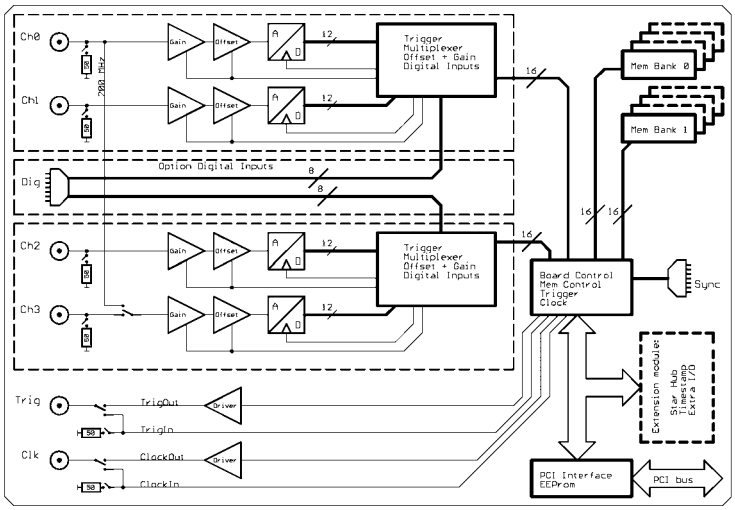
Model	1 channel	2 channels	4 channels
MI.3010	80 MS/s		
MI.3011	40 MS/s	40 MS/s	
MI.3012	80 MS/s	40 MS/s	
MI.3013	40 MS/s	40 MS/s	40 MS/s
MI.3014	80 MS/s	80 MS/s	40 MS/s
MI.3015	160 MS/s	80 MS/s	
MI.3016	160 MS/s	80 MS/s	40 MS/s
MI.3020	100 MS/s		
MI.3021	50 MS/s	50 MS/s	
MI.3022	100 MS/s	50 MS/s	
MI.3023	50 MS/s	50 MS/s	50 MS/s
MI.3024	100 MS/s	100 MS/s	50 MS/s
MI.3025	200 MS/s	100 MS/s	
MI.3026	200 MS/s	100 MS/s	50 MS/s
MI.3027	100 MS/s	100 MS/s	
MI.3031	60 MS/s	60 MS/s	
MI.3033	60 MS/s	60 MS/s	60 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2(as option)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

Hardware block diagram



Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock
Input Range	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±100% in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/256 to 255/256 of input range
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

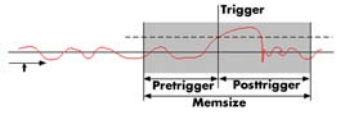
Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscopie	Test of mobile communication
Ultrasound	Medical equipment	Sonar

SPECTRUM SYSTEMENTWICKLUNG MICROELECTRONIC GMBH · AHRENSFELDER WEG 13-17 · 22927 GROSSHANSDORF · GERMANY
PHONE: +49 (0)4102-6956-0 · FAX: +49 (0)4102-6956-66 · E-MAIL: info@spec.de · INTERNET: http://www.spec.de

Possibilities and options

Input impedance
All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode


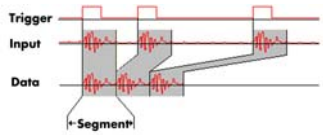
The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording in a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

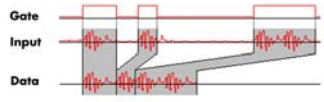
Channel trigger
The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes could be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

External trigger I/O
All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulsewidth. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

Pulse width
Defines the minimum or maximum width that a trigger pulse could have to generate a trigger event. Could be combined with channel trigger, pattern trigger and external trigger.

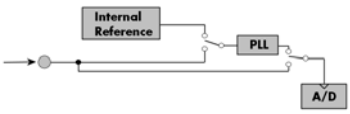
Multiple Recording


The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

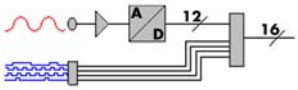
Gated Sampling


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O
Using an external connector a sampling clock could be fed in from an external system. It's also possible to put out the internally used sampling clock to synchronise external equipment to this clock.

Reference clock


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

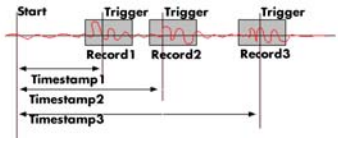
Digital inputs


This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

Cascading
The cascading option synchronises up to 4 Spectrum boards internally. It's the simpliest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

Star hub
The star hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and could be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that could be used directly at the rear board connector.

Timestamp


The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relatively to the start of recording, to a defined zero time or externally synchronised to a radio clock or a GPS receiver. With this option acquisitions of systems on different locations could be set in a precise time relation.

Technical Data

Resolution	12 bit	Input signal with 50 Ohm termination	max 5 V rms
Differential linearity error	≤ 1 LSB (ADC)	Input impedance	50 Ohm / 1 MOhm || 25 pF
Integral linearity error	≤ 1 LSB (ADC)	Overvoltage protection (range ≤ ±1 V)	±5 V
Offset error	adjustable by user	Overvoltage protection (range > ±1 V)	±50 V
Gain error	< 1%	Digital Inputs input impedance	110 Ohm @ 2.5 V
Crosstalk 1 MHz signal, 50 Ohm term	< -70 dB	Digital Inputs delay to analog sample	-12 samples
Multi: Trigger to 1st sample delay	-10 to +20 samples (fix)	Dimension	312 mm x 107 mm
Multi: Recovery time	< 20 samples	Width (Standard)	1 full size slot
ext. Trigger accuracy (<125 MS/s)	1 Samples	Width (with digital inputs or star hub)	1 full size slot and 1 half size slot
ext. Trigger accuracy (>160 MS/s)	2 Samples	Connector	3 mm SMB male
int. Trigger accuracy	1 Sample	Warm up time	10 minutes
Trigger output delay		Operating temperature	0°C - 50°C
		Storage temperature	-10°C - 70°C
Ext. clock: delay to internal clock	42 ns ± 2 ns	Humidity	10% to 90%
Min internal clock	1 kS/s	Power consumption 5 V @ full speed	max 3.4 A (17.0 Watt)
Min external clock	1 MS/s	Power consumption 5 V @ power down	max 2.3 A (11.5 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge is used. Required duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA)

Dynamic Parameters

	MI.3011 MI.3013	MI.3021 MI.3023	MI.3031 MI.3033	MI.3010 MI.3012 MI.3014	MI.3020 MI.3022 MI.3024 MI.3027	MI.3015 MI.3016	MI.3025 MI.3026
max internal clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	160 MS/s	200 MS/s
max external clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
-3 dB bandwidth	> 20 MHz	> 25 MHz	> 30 MHz	> 40 MHz	> 40 MHz	> 40 MHz	> 40 MHz
Zero noise level (< 125 MS/s)	< 1.5 LSB rms	< 1.5 LSB rms	< 1.75 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms
Zero noise level (> 125 MS/s)	n.a.	n.a.	n.a.	n.a.	n.a.	< 3.0 LSB rms	< 3.0 LSB rms
Test - Samplerate	40 MS/s	50 MS/s	60 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
Testsignal frequency	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz
SNR (typ)	>65.5 dB	>65.5 dB	>63.7 dB	>65.3 dB	>65.1 dB	>65.3 dB	>63.9 dB
THD (typ)	<-74.5 dB	<-74.5 dB	<-73.6 dB	<-74.5 dB	<-74.5 dB	<-74.3 dB	<-74.0 dB
SFDR (typ), excl harm.	>79.5 dB	>79.5 dB	>74.3 dB	>79.1 dB	>78.8 dB	>79.0 dB	>75.3 dB
SINAD (typ)	>64.7 dB	>64.7 dB	>63.3 dB	>64.8 dB	>64.5 dB	>64.8 dB	>63.5 dB
ENOB (based on SINAD)	>10.5	>10.5	>10.2	>10.5	>10.4	>10.5	>10.3

Dynamic parameters are measured at ± 1 V input range and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MI3010	MI.3010 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MI3011	MI.3011 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MI3012	MI.3012 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
MI3013	MI.3013 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-128M	Option: 128 MSample memory instead of 8 MSample standard mem
MI3014	MI.3014 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-256M	Option: 256 MSample memory instead of 8 MSample standard mem
MI3015	MI.3015 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-up	Additional handling costs for later memory upgrade
MI3016	MI.3016 with 8 MSample memory and drivers/SBench 5.x		
MI3020	MI.3020 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-mr	Option Multiple Recording: Memory segmentation
MI3021	MI.3021 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-gs	Option Gated Sampling: Gate signal controls acquisition
MI3022	MI.3022 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-dig	Additional 4 synchronous digital inputs per channel, incl. cable
MI3023	MI.3023 with 8 MSample memory and drivers/SBench 5.x	MI3xxx-cs	Synchronisation of 2 - 4 boards, one option per system
MI3024	MI.3024 with 8 MSample memory and drivers/SBench 5.x	MI.30xx-hbw	100 MHz bandwidth for MI.3025/26 at fixed ±500 mV input
MI3025	MI.3025 with 8 MSample memory and drivers/SBench 5.x	MI30xx-dl	DASYLab driver for MI.30xx series
MI3026	MI.3026 with 8 MSample memory and drivers/SBench 5.x	MI30xx-hp	VEE driver for MI.30xx series
MI3027	MI.3027 with 8 MSample memory and drivers/SBench 5.x	MI30xx-lv	LabVIEW driver for MI.30xx series
MI3031	MI.3031 with 8 MSample memory and drivers/SBench 5.x	MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.
MI3033	MI.3033 with 8 MSample memory and drivers/SBench 5.x		
MI3xxx-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	MI3xxx-time	Timestamp option: Extra memory for trigger time
MIxxxx.xio	Extra I/O, internal connector: 16 DI/O, 4 Analog out	MIxxxx-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm

technical changes and printing errors possible